Amendments to the Specification:

Please replace the Abstract with the following amended version:

ABSTRACT

A memory architecture for a non-volatile analog or multiple-bits-per-cell memory includes multiple separate memory arrays and multiple read/write pipelines. The multiple read/write pipelines share a read circuit and/or a write circuit to reduce the circuit area of each pipeline and the circuit area of the memory as a whole. In one embodiment, a shared write circuit generates a programming voltage that changes with an input signal representing values to be written to the memory. Each pipeline includes a sample-and-hold circuit that samples the programming voltage when the pipeline begins a write operation. The write circuit can additionally generate a verify voltage that a second sample-and-hold circuit in each pipeline samples when starting a write operation. ~~In another embodiment, a shared read circuit generates a read signal that ramps across the range of permitted threshold voltages for the memory cells, and a sense amplifier in each pipeline clocks a sample-and-hold circuit or another temporary storage circuit when the sense amplifier senses a transition in conductivity of a selected memory cell. When clocked, the sample-and-hold circuit or other temporary storage circuit registers a signal that corresponds to the read signal and indicates a data value associated with the voltage of the read signal. In alternative embodiments, the signal registered is the read signal, a converted form of the read signal, or a multi-bit digital signal.~~